

**RESOLUTION Project**  
**IST - 026851****Design of reflector on advanced CMOS**  
**[D9]**

---

**Document Information**

---

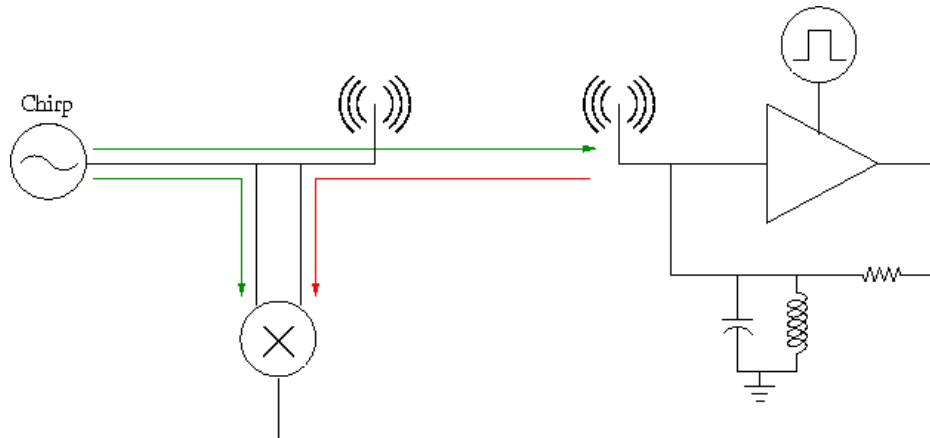
<b>Title</b>	D9 – Design of reflector on advanced CMOS
<b>Workpackage</b>	WP 4 – CMOS System
<b>Responsible</b>	ETH Zürich
<b>Due Date</b>	Project Month 18 (July 2007)
<b>Type</b>	Report
<b>Status</b>	Version 1.0
<b>Security</b>	Public
<b>Authors</b>	Silvan Wehrli
<b>Project URL</b>	<a href="http://www.ife.ee.ethz.ch/RESOLUTION/">http://www.ife.ee.ethz.ch/RESOLUTION/</a>

---

## Table of contents

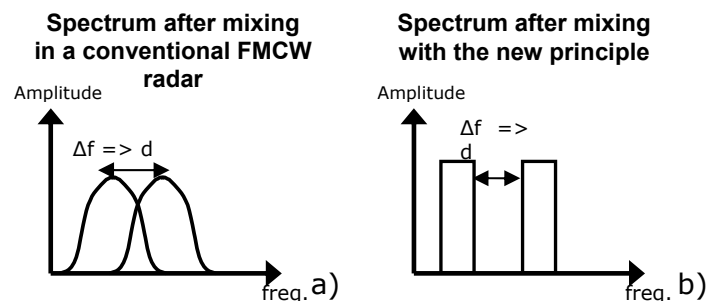
<b>TABLE OF CONTENTS</b>	<b>2</b>
<b>1 INTRODUCTION</b>	<b>3</b>
<b>2 THEORETICAL ANALYSIS OF THE ALPR PRINCIPLE</b>	<b>4</b>
2.1 PHASE COHERENT START-UP OF THE REFLECTOR	5
2.2 SIMULINK SIMULATIONS OF THE ALPR	7
<b>3 ARCHITECTURE OF FIRST PROTOTYPE AND SIMULATION RESULTS</b>	<b>9</b>
3.1 ARCHITECTURE OF THE REFLECTOR	9
3.1.1 LOW NOISE AMPLIFIER	10
3.1.2 SINGLE-ENDED TO DIFFERENTIAL CONVERSION	10
3.1.3 DIFFERENTIAL TO SINGLE-ENDED CONVERSION	11
3.2 POST LAYOUT SIMULATIONS	12
3.3 LAYOUT	14
<b>4 ON-WAFER MEASUREMENT RESULTS</b>	<b>15</b>
4.1 MEASUREMENT RESULTS	15
4.2 CONCLUSION AND OUTLOOK	16
<b>5 PCB DESIGN</b>	<b>17</b>
<b>6 AUTO CALIBRATION CIRCUIT</b>	<b>18</b>
6.1 COMPARISON OF DIFFERENT SELF CALIBRATION SCHEMES	18
6.1.1 VARACTOR TUNING	18
6.1.2 PLL	19
6.1.3 ALL-DIGITAL PLL	19
6.2 COMPARISON OF CALIBRATION METHODS	19
6.3 CONCEPT OF AUTO CALIBRATION USING AN ADPLL	20
6.4 ESTIMATED POWER CONSUMPTION AND AREA OF AN ADPLL	20
6.5 FIRST SIMULATION RESULTS	20
<b>7 CONCLUSION</b>	<b>21</b>
<b>8 REFERENCES</b>	<b>21</b>

# 1 Introduction



**Fig. 1. Local positioning RADAR system using a pulsed active reflector. The transmitter sends a frequency ramp out. The reflector regenerates the phase and transmits the signal back. In the base station, the received and the transmitted signal is mixed down and filtered.**

To localize an object a passive or active reflector is needed. The RESOLUTION project uses an active reflector to achieve the large localization range of 200m, which is required by the specifications. Siemens has patented a new Radar system called ALPR (Advanced Local Positioning Radar) to further improve the predicted accuracy to the centimetre regime [1]. A conventional reflector only amplifies the received signal. This new reflector approach uses a pulsed active reflector. The received signal excites an oscillation at the resonance frequency of the reflector. This oscillation has initially the same phase as the incoming signal. Due to the different frequencies the phase difference between the two signals will increase over time. The reflector is switched on and off after 40ns to resynchronise the phase. By switching the reflector on and off, the edges in the spectrum get steeper and are therefore easier to detect as can be seen qualitatively in Fig. 2b. A mathematical derivation can be obtained in [1]. Furthermore, the SNR is improved by regenerating the oscillation instead of just amplifying it.



**Fig. 2. This qualitative illustration shows the spectrum after mixing down. a) shows the spectrum of a conventional FMCW system and b) the spectrum of the ALPR system.**

The remainder is organised as follows. In the second section of the deliverables report a mathematical derivation of the active pulsed reflector approach is discussed. The main principle is explained and special attention lies on the phase

coherent start-up of the reflector. The analytical derivations are verified with Matlab and Simulink simulations. In the third section, the architecture of the first prototype is presented. The measurement results of the first prototype are listed in the fourth section. The fifth section goes into the design of the test board. At the end of this report, an outlook to future improvements is given.

## 2 Theoretical analysis of the ALPR Principle

A RADAR system measures the distance of an object to the receiver. This can be done by passive reflections on the object, as this is the case for airplane RADARS. An active reflector can be used to enhance the measurement range. It amplifies the incoming signal and sends it back. The drawback of a simple active reflector is that the noise is also amplified and even some noise is added in the amplifier. The novel pulsed active reflector prevents the noise from being amplified by regenerating the signal. The active pulsed reflector is switched on and off with a pulse frequency. Every time the reflector is switched on, the reflector starts to oscillate with the same phase as the incoming signal, but oscillates with its own resonance frequency  $\omega_o$ . The following calculation demonstrates how the distance can be calculated from the mixing product of the transmitted and the received signal.

The base station sends a frequency ramp to the reflector. The frequency ramp has a constant frequency  $\omega_B$  and a time dependent part  $\omega_{SW}$  with the initial phase  $\phi_0$ :

$$s_{tx} = \cos\left((\omega_B + \omega_{SW})t + \phi_0\right) \quad (1)$$

The phase at the reflector is then

$$\phi_i = \phi_0 - (\omega_B + \omega_{SW})\tau \quad (2)$$

where  $\tau/2$  depicts the time of flight from the base station to the reflector. The phase coherent reflector sends the following signal back

$$s_o = \cos\left(\omega_o\left(t + \frac{\tau}{2}\right) + \phi_0 - (\omega_B + \omega_{SW})\tau\right) \quad (3)$$

This signal is sent to the base station and therefore a delay of another  $\tau/2$  is added. The received signal equals

$$s_{rx} = \cos\left(\omega_o t + \phi_0 - (\omega_B + \omega_{SW})\tau\right) \quad (4)$$

To simplify the calculations, one can assume that the centre frequency of the swept signal is equal to the resonance frequency. The received signal is mixed with the sent signal:

$$\begin{aligned} s_{mix} &= \cos\left((\omega_0 + \omega_{SW})t + \phi_0\right) \times \cos\left(\omega_0 t + \phi_0 - (\omega_0 + \omega_{SW})\tau\right) \\ &= \frac{1}{2} \cos\left((2\omega_0 + \omega_{SW})t + 2\phi_0 - (\omega_0 + \omega_{SW})\tau\right) + \frac{1}{2} \cos\left(\omega_{SW}t + (\omega_0 + \omega_{SW})\tau\right) \end{aligned} \quad (5)$$

After low pass filtering, which has the effect of an integration over one interval when the reflector is on, the signal looks as follow.

$$s_{dc} = 2 \cos\left((\omega_0 + \omega_{SW})\tau + \frac{1}{2}T_s\omega_{SW}\right) \frac{\sin\left(\frac{1}{2}T_s\omega_{SW}\right)}{\omega_{SW}} \quad (6)$$

Substituting  $\omega_{sw}$  with  $\omega_{sw} = (4\pi Bt)/T - \pi B$  gives the final equation for the down mixed and filtered signal.

$$s_{dc} = \cos\left(t\left(\frac{4\pi B\tau}{T} + \frac{2\pi B T_s}{T}\right) + (\omega_0 - \pi B)\tau + \frac{1}{2}T_s\pi B\right) \frac{\sin\left(\frac{1}{2}T_s\left(\frac{4\pi Bt}{T} - \pi B\right)\right)}{\frac{4\pi Bt}{T} - \pi B} \quad (7)$$

Equation (7) is a cosine wave modulated with a sinc function. The frequency of the cosine function is proportional to the delay between the sent and the reflected signal, therefore the distance between the active pulsed reflector and the base station can be calculated. The resonance frequency of the reflector does not influence the frequency of the down mixed signal. Thus the resonance frequency of the reflector does not have to be very precise.

### 2.1 Phase Coherent Start-Up of the Reflector

The active pulsed reflector approach works only, if the reflector starts to oscillate with the same phase as the incoming signal. This phase coherent start-up was analytically calculated using a simple reflector model depicted in Fig. 3.

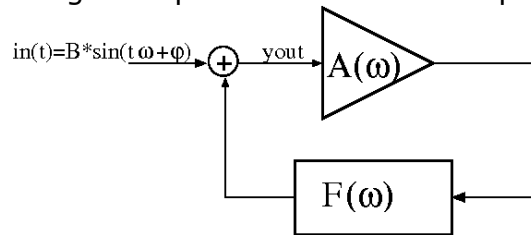


Fig. 3. Simple reflector used for the theoretic analysis.

The transfer function of the band pass filter is defined by the quality factor  $Q$  and the pass frequency  $\omega_0$

$$F_{Filt} = \frac{\frac{\omega_0}{Q} s}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \quad (8)$$

The reflector receives an incoming sine wave

$$in(t) = B \cdot \sin(\omega t + \varphi_0) \quad (9)$$

Calculations in the Laplace domain derived the output signal of the reflector:

$$y_{out} = x \cdot \sin(\omega t + \varphi_0) + y \cdot \cos(\omega t + \varphi_0) + q \cdot e^{\frac{A\omega_0}{2Q} t} (u \cdot \sin(\omega_0' t) + v \cdot \cos(\omega_0' t)) \quad (10)$$

As stated in [1] the reflector should start with its self resonance frequency instead of the frequency of the incoming wave. From (10), it can be shown that two conditions (11)(12) have to be satisfied to guarantee this behaviour:

$$4Q^2 > A^2 \quad (11)$$

$$\frac{A\omega_0}{2Q} > 0 \quad (12)$$

The oscillation at the resonance frequency grows exponentially and is the dominant influence on the phase. The terms  $u$  and  $v$  are given by

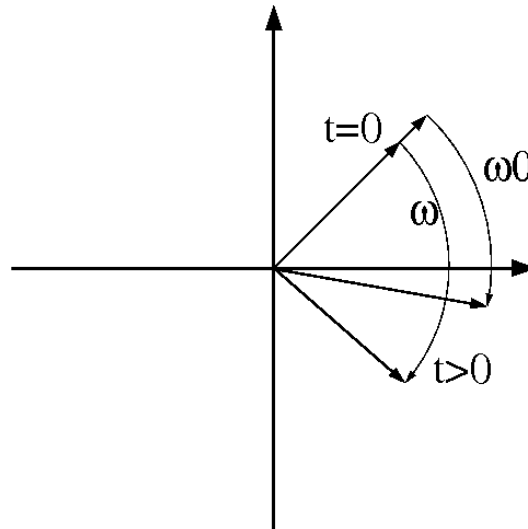
$$u(\varphi_0) = Q\omega A(\omega^2 + \omega_0^2) \cos \varphi_0 + A^2 \omega^2 \sin \varphi_0 + 2Q^2 \omega_0 (\omega_0^2 - \omega^2) \sin \varphi_0 \quad (13)$$

$$v(\varphi_0) = \sqrt{|A^2 - 4Q^2|} \omega \left( Q(\omega^2 - \omega_0^2) \cos \varphi_0 + A\omega_0 \omega \sin \varphi_0 \right) \quad (14)$$

The starting phase of the oscillation is calculated by

$$\varphi = \text{angle}(u + i \cdot v) \quad (15)$$

Illustration Fig. 4 shows the behaviour of the phasors of the incoming wave and the reflected wave. When the reflector is switched on, an oscillation is generated which has the same starting phase as the incoming wave. The phasors rotate with different frequencies and, therefore, the phase difference between the two signals increases over time.



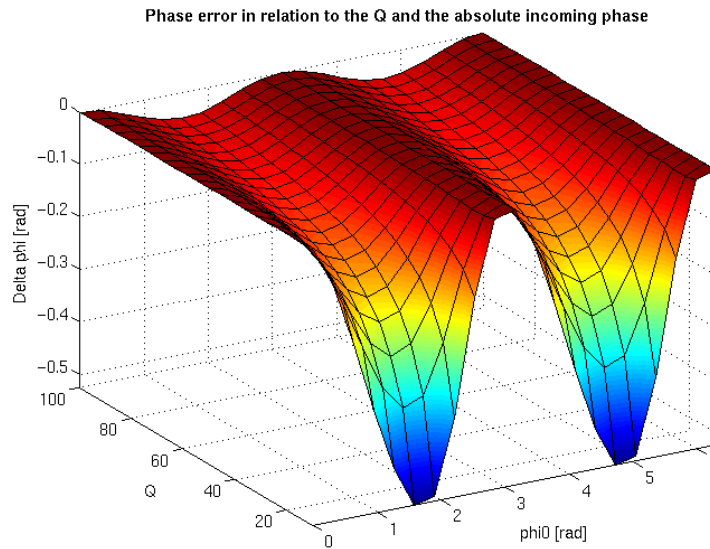
**Fig. 4. Phasor illustration of the incoming wave and the reflected wave.**

The Matlab simulation of the phase error at the beginning of the oscillation for different quality factors  $Q$  and  $\varphi_0$  is plotted in Fig. 5.

Two interesting behaviours can be observed: The phase error at the beginning of the oscillation is dependent on the phase of the incoming wave. The smallest error occurs for  $\varphi_0 = k \cdot \pi$  ( $k=0,1,2,\dots$ ) and the largest error for  $\varphi_0 = k \cdot \pi + \pi/2$  ( $k=0,1,2,\dots$ ). Due to the integration process during one measurement, this phase error is averaged and roughly constant. This helps reducing the affect on the accuracy of the system. The value of the phase error is also dependent on the ratio  $Q/A$ . For a small phase error a high  $Q$ -factor is needed. This can also be seen in the formulas for  $u$  and  $v$ . If the quality factor of the loop filter  $Q$  is much larger than the gain  $A$  and  $\omega$  is equal to  $\omega_0$ ,  $u$  and  $v$  can be simplified to

$$\begin{aligned} u(\varphi_0) &\approx 2QA\omega^3 \cos \varphi_0 \\ v(\varphi_0) &\approx 2QA\omega^3 \sin \varphi_0 \end{aligned} \quad (16)$$

Substituting (16) in (15) reveals that the starting phase is perfectly preserved. The oscillating frequency  $\omega_0'$  is equal to the resonance frequency  $\omega_0$ .



**Fig. 5. Phase error in relation to the quality factor  $Q$  of the filter in the reflector and to the phase of the incoming signal for a constant loop gain  $A=5$ .**

## 2.2 Simulink Simulations of the ALPR

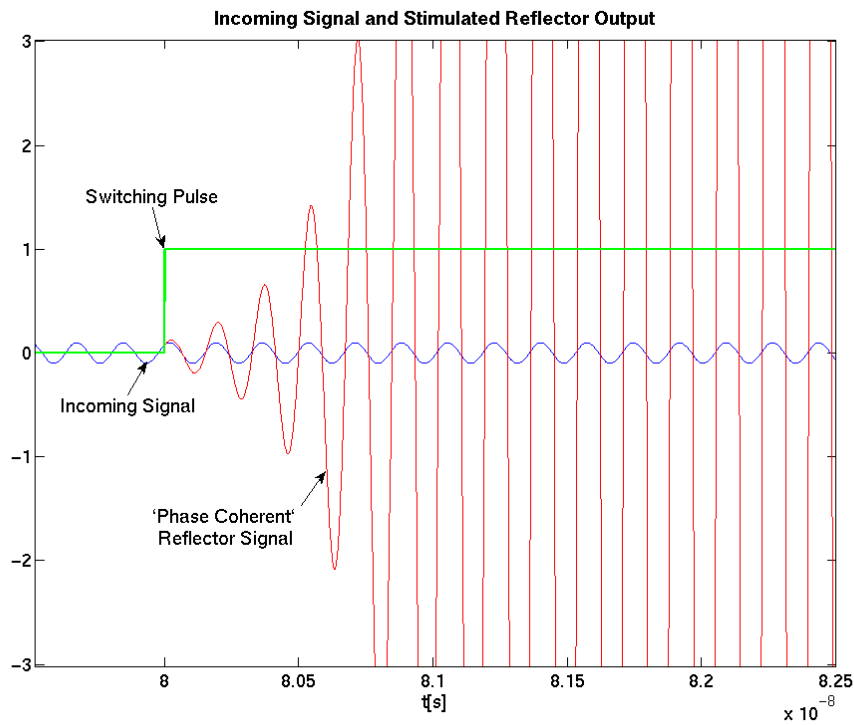
To verify the functionality of the ALPR system, a simplified system has been build up in Simulink. The transmitter of the base station (BS) sends a FMCW-signal (frequency modulated continuous wave) over the channel to the reflector. After the reflector has transmitted the signal back through the channel, the receiver in the BS mixes the signal down and filters it. The channel is modelled as a delay element and an attenuator in series. The mixer is a simple multiplier and the filter has a second order low pass characteristic.

With this Simulink model it is possible to compare a simple state-of-the-art reflector with the more advanced ALPR reflector. Both reflectors are modelled using ideal amplifiers and lumped elements, e.g. resistors, capacitance and inductance.

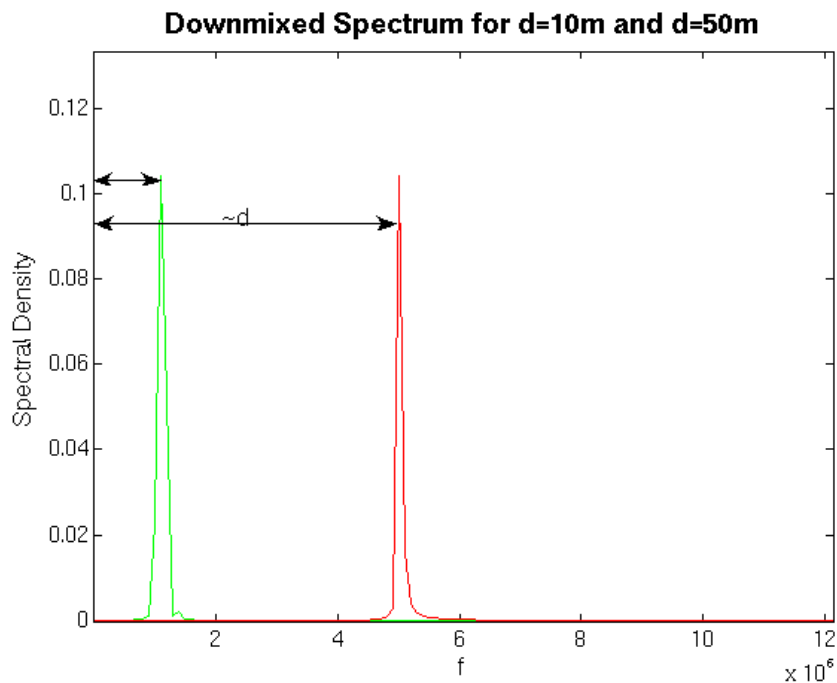
The Simulink model shows that the reflector starts phase coherent to the incoming signal. This can be seen in Fig. 6. For the simulation a realistic gain of 10 and a quality factor  $Q$  of 16 were chosen.

The normalized spectrum (main peak=1) of the down mixed received signal is shown in Fig. 7. Both the ALPR and the FMCW system have the main peak at the same frequency.

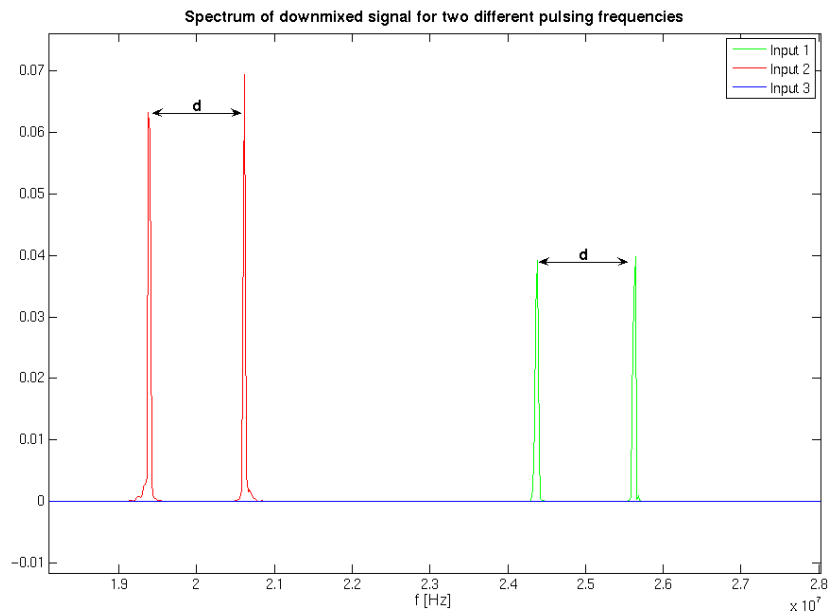
Due to the pulsing of the reflector the ALPR spectrum shows mirrored frequencies. The switching on and off of the reflector is equal to a modulation of the reflected signal with a square wave. With this modulation, passive reflected signals can be distinguished from the desired active reflected signals. Furthermore, different reflectors can be identified by the modulation frequency as depicted in Fig. 8.



**Fig. 6.** The reflector starts with the same phase as the incoming signal. Due to the different frequencies the two phases diverge.



**Fig. 7.** Normalized spectrum after mixing for a conventional active reflector (FMCW) and a novel pulsed reflector (ALPR).



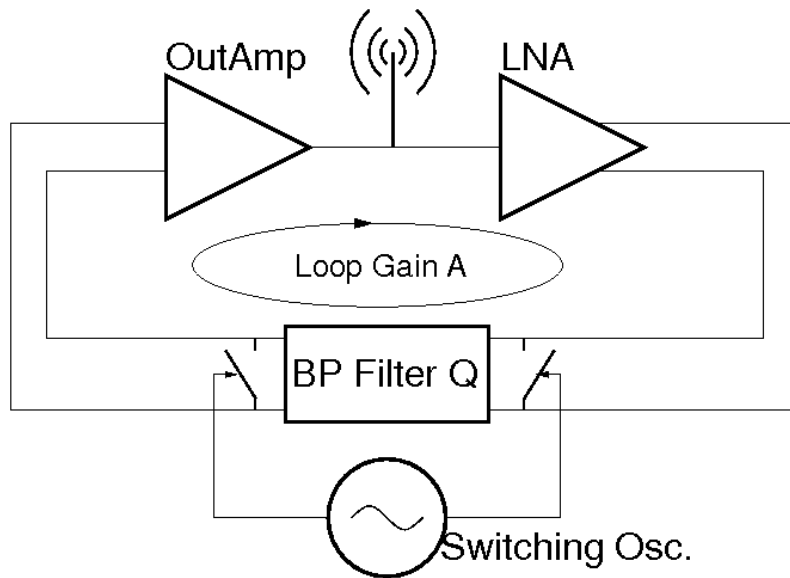
**Fig. 8. Spectrum of the down mixed signal of the RADAR system using an active pulsed reflector. The red curve shows the signal for a switching frequency of 20MHz and the green signal of 25MHz.**

### 3 Architecture of first Prototype and Simulation Results

The analysis of the active pulsed reflector revealed some important trade-offs. A high loop gain allows a fast oscillation start-up. But the loop gain has to be smaller than  $2Q$ . The reflectors must be switched on and off. The switching of the reflector disturbs the phase coherent start-up of the reflector. The influence of the switching can be minimized by shortening differential signals. Thus a differential loop filter together with a single ended to differential and a differential to single ended conversion is implemented.

#### 3.1 Architecture of the Reflector

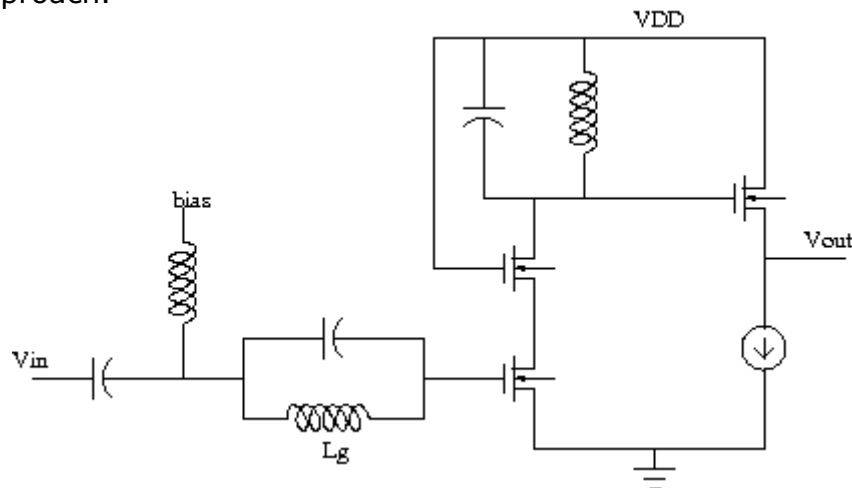
The reflector consists of a LNA at the input, followed by a conversion from single ended to differential. The reflector is switched off by shortening the differential signals before and after the filter. The differential signal is then transformed back and amplified with a PA. This signal is fed back to the LNA. The incoming signal leads to a phase coherent, autonomous oscillation.



**Fig. 9. Overall reflector topology.**

### 3.1.1 Low Noise Amplifier

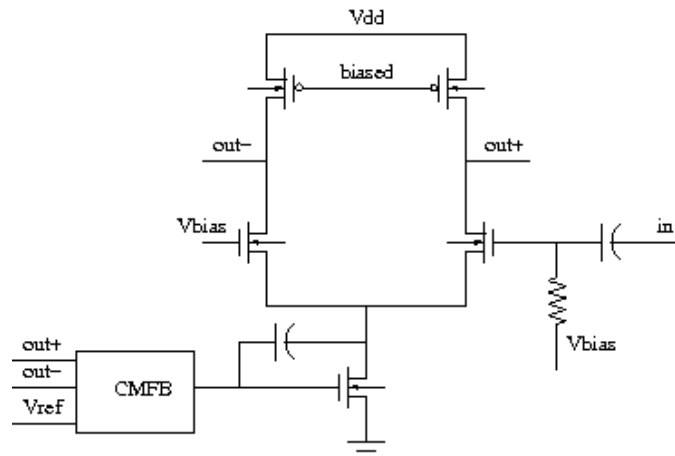
The noise figure of a circuit is dominated by the first stage. This is ideally a low noise amplifier (LNA). A cascaded common source approach was chosen for the LNA. This LNA was proposed in [2]. The structure is depicted in Fig. 10. The advantage of this approach is that no source degeneration is used. The parallel LC structure transforms the parasitic resistance of the inductor to a larger resistance which makes matching easier. A simulated NF of 3.3dB was achieved with this approach.



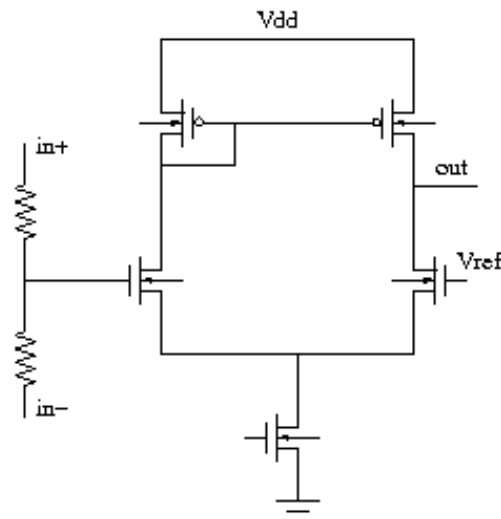
**Fig. 10. Common source LNA structure**

### 3.1.2 Single-Ended to Differential Conversion

The single ended to differential converter transforms the output of the LNA to a differential signal for the filter. A differential signal has the advantage of the higher supply noise rejection. By shortening the differential signals, the reflector can be simply switched on and off. For the conversion a differential pair with common mode feedback (CMFB) is used. The common mode output voltage can be set to a wanted reference voltage. The CMFB allows an increased output swing. A Miller capacitance had to be introduced to stabilize the CMFB.



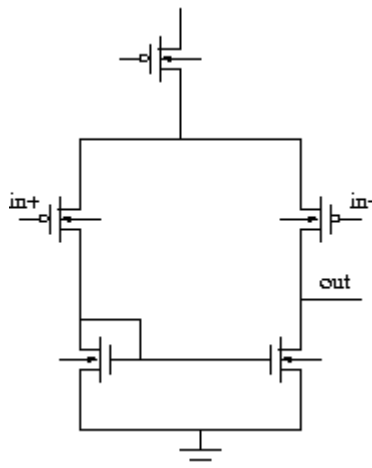
**Fig. 11. Single ended to differential conversion with CMFB for a higher output swing.**



**Fig. 12. Common mode feedback (CMFB) for the single ended to differential conversion.**

### 3.1.3 Differential to Single-Ended Conversion

One goal was to keep the chip size small. This could be achieved by designing the differential to single ended conversion so, that the PA does not need a separate bias voltage. A PMOS input pair was chosen to achieve a low output voltage of 0.6V at the differential to single ended conversion as shown in Fig. 13.



**Fig. 13. Differential to single ended conversion using a simple PMOS input pair.**

### 3.2 Post Layout Simulations

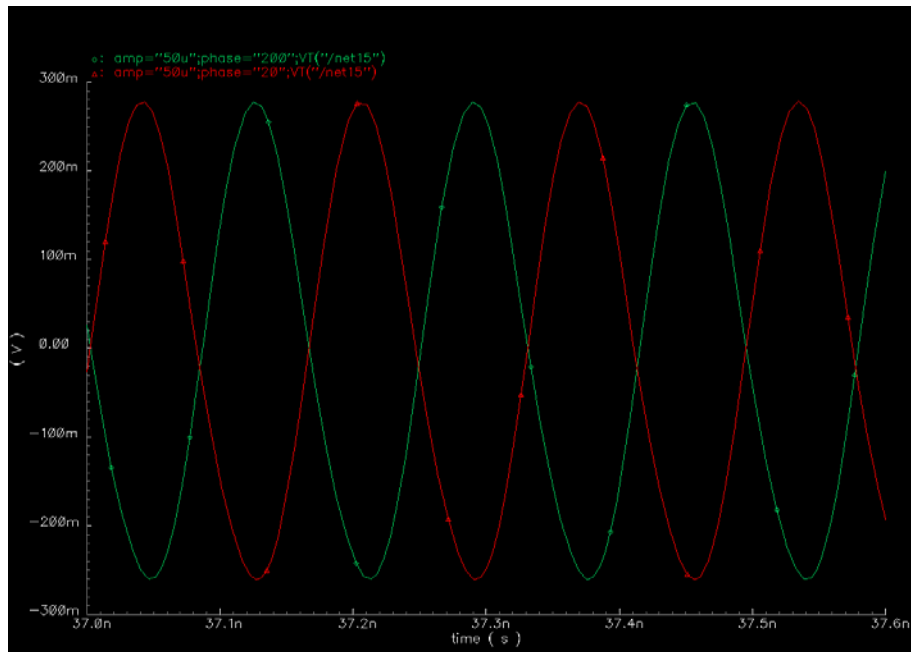
The correct functionality of the reflector was verified with an RC extraction of the layout.

The sensitivity was simulated by applying two 180° shifted input signals. If the reflector starts phase coherent, then the phase difference between the two excited signals always has to be 180°. The two reflected output signals are plotted in Fig. 14. An input sensitivity of -75dBm was simulated. The real sensitivity is going to be smaller due to noise and distortion by channels close to the wanted frequency. The high sensitivity was achieved by a small loop gain and small switching transistors, because the switching on pulse is then less amplified. The drawback of a small loop gain is the long start-up time as can be seen in Fig. 15.

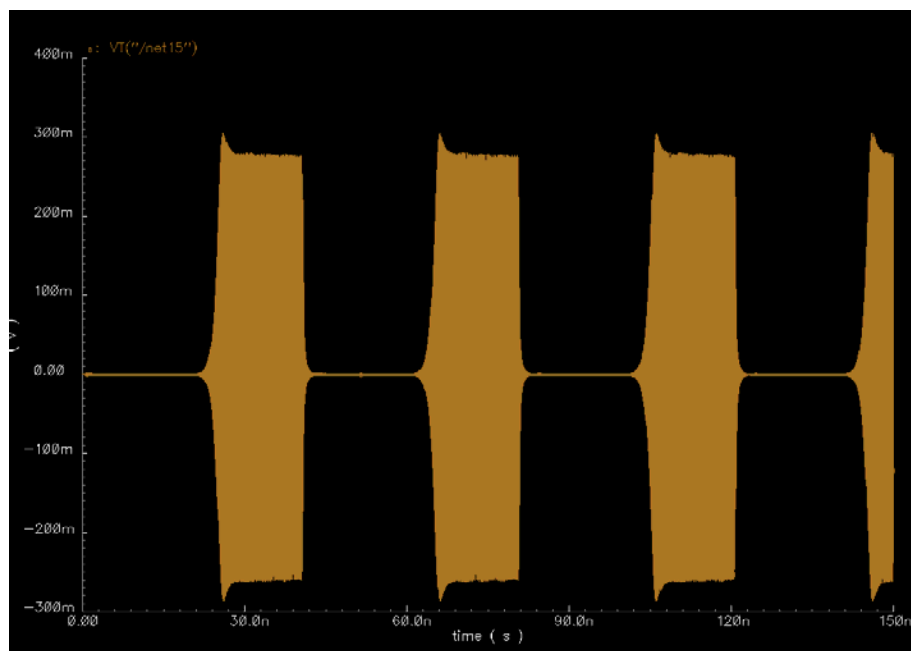
The output power decreased from schematic simulations to post layout simulations due to the parasitic capacitances and resistors. Schematic simulations showed an output power of up to 2mW. In post layout simulations only 0.73mW could be achieved.

Parameter	Simulated
Loop gain A	10=20dB
Quality factor Q	17
Resonance frequency	6GHz
Output power	0.73mW
Power consumption	52mW oscillating, 27mW not osc.
Area	1x1mm <sup>2</sup>
Sensitivity	-75dBm

**Tab. 1. Extracted simulation results of the active pulsed reflector.**



**Fig. 14 Phase coherent oscillation (input signal is only 0.05mV)**



**Fig. 15. The reflector is switched on and off with a 25MHz square wave.**

### 3.3 Layout

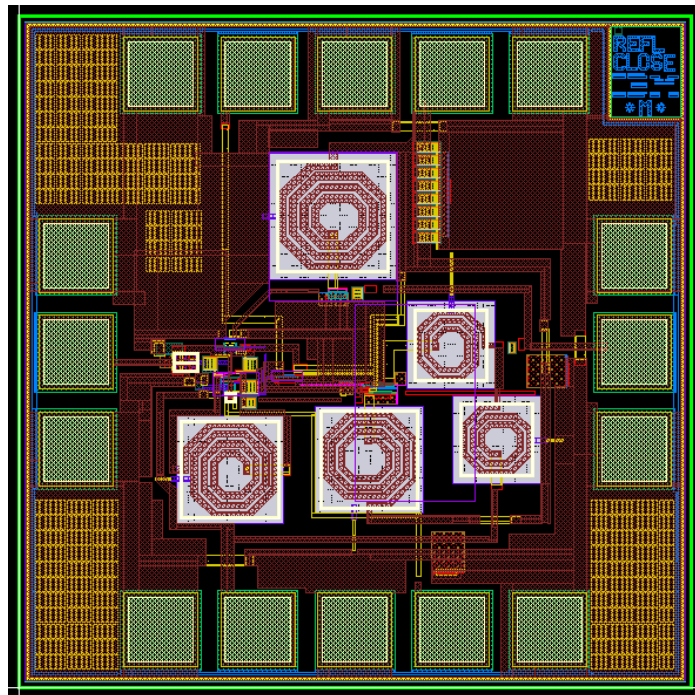


Fig. 16. Chip layout of the active pulsed reflector measures 1x1mm<sup>2</sup>.

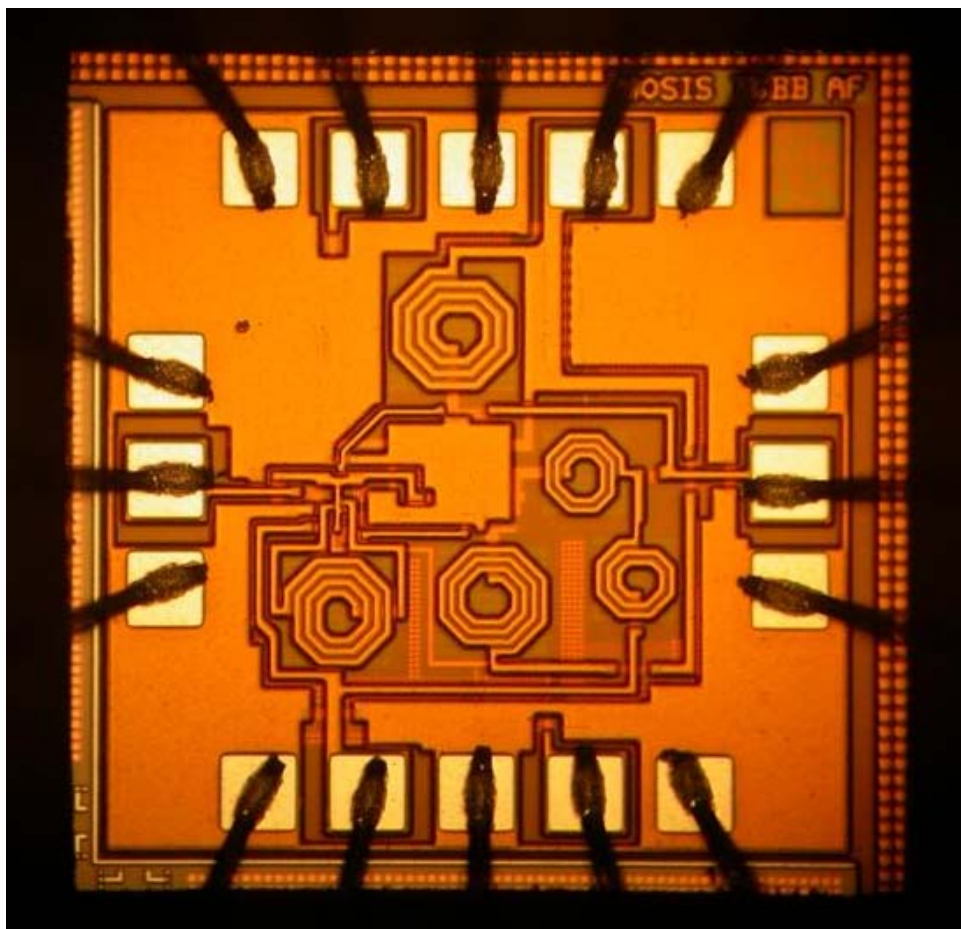


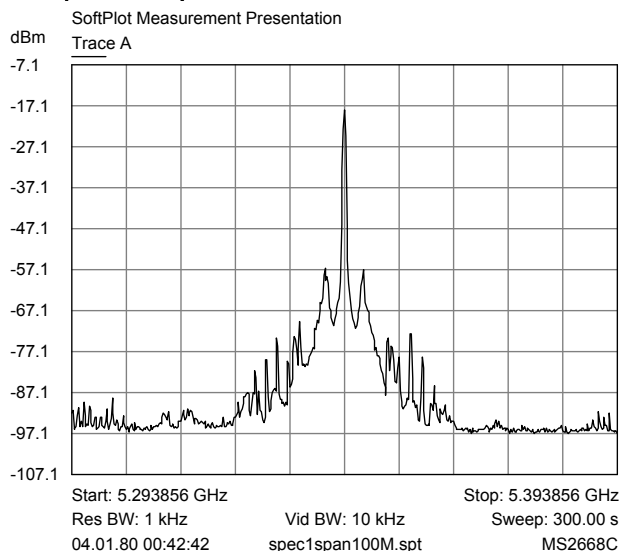
Fig. 17. Microphotograph of the integrated reflector bonded on the PCB.

## 4 On-wafer measurement results

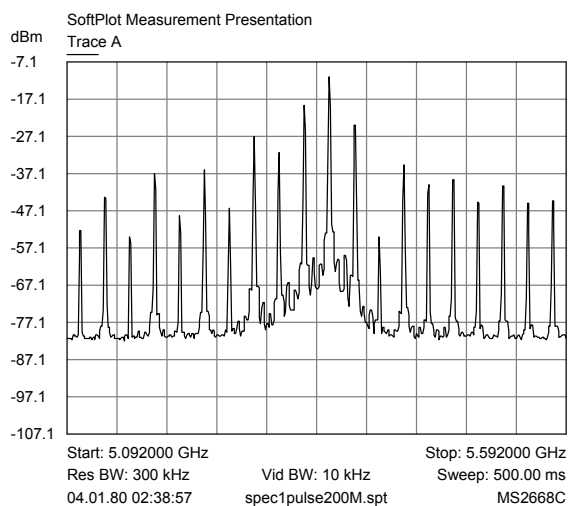
### 4.1 Measurement Results

The fabricated reflector has been measured and characterised. The spectrum of the free running reflector can be seen in Fig. 18. The reflector does oscillate, but only at 5.35GHz instead of 5.8GHz. This frequency deviation is probably caused by production variations. The centre frequency of the reflector is not perfectly stable due to its free running nature. The transmitted power in a 1MHz band is 0.23dBm, which corresponds rather well with the simulation results of -1.023dBm.

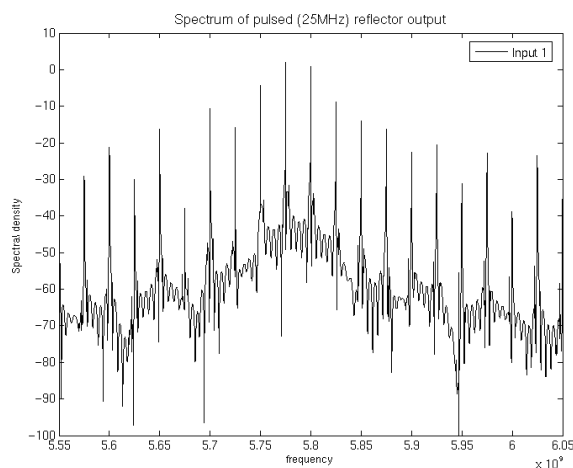
In Fig. 19 the pulsing capability of the reflector is illustrated. The reflector is pulsed with a 25MHz square wave. The measured spectrum, plotted in Fig. 19a, matches the Matlab simulation results shown in Fig. 19b. The reflector can also be pulsed with higher frequencies. The spectrum for a pulse frequency of 200MHz is shown in Fig. 20. The phase noise at 1MHz and 20MHz offset are -70dBc and -107dBc respectively.



**Fig. 18. Spectrum of the free running reflector.**



(a)



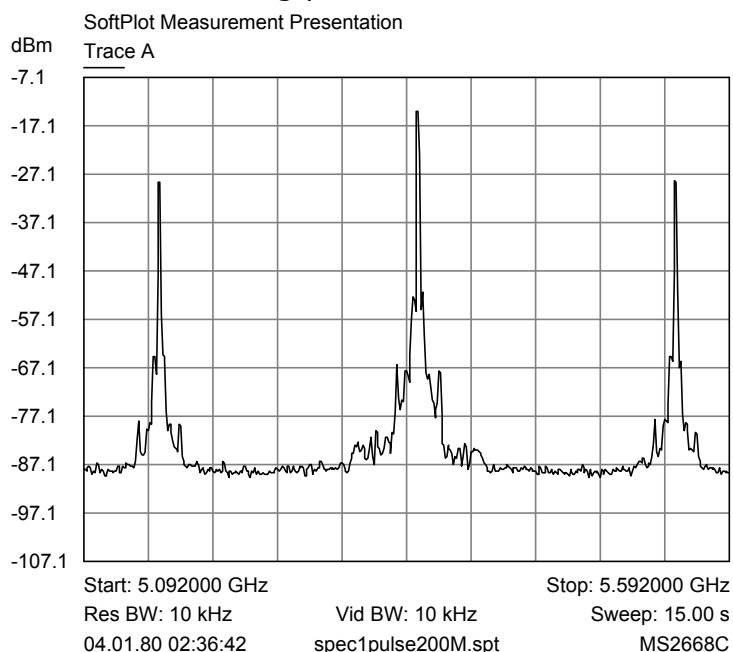
(b)

**Fig. 19. Comparison of the spectrum of the pulsed reflector: measurement and Matlab simulation.**

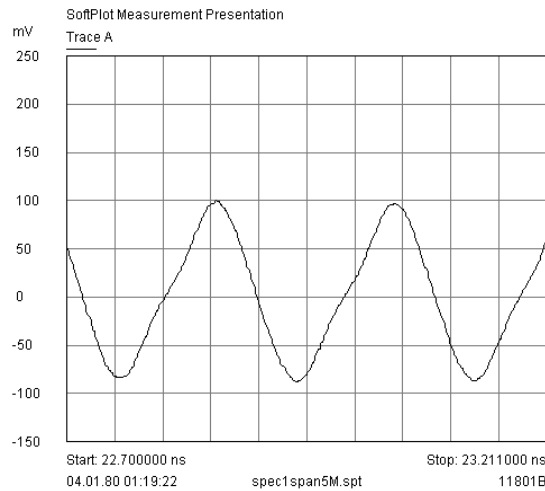
The oscillation is not perfectly symmetrical. The rising edge is slower than the falling edge as depicted in Fig. 21. A fully differential architecture would prevent this asymmetric at the cost of an external balun.

### 4.2 Conclusion and Outlook

The measurements match fine with the simulation results. The main difference is the too low resonance frequency. The resonance frequency can be tuned via the bias voltages to a higher frequency, but the amplitude does further reduce. This shows that the frequency is too low because of the passive elements of the loop filter. Therefore, the reflector needs to be adaptable and the filter has to be made tuneable. Different tuning possibilities are discussed in section 6.



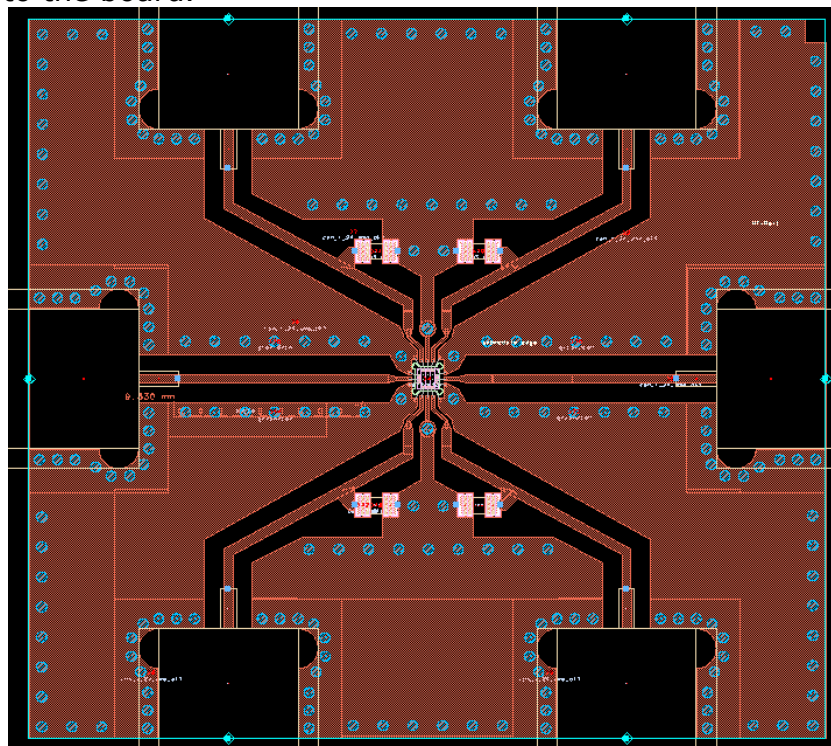
**Fig. 20. Reflector pulsed with 200MHz.**



**Fig. 21. Reflector output: Amplitude smaller than 1/2 of the effective amplitude due to power splitter in the measurement setup.**

## 5 PCB Design

This part describes the design of the printed circuit board (PCB) used for testing the integrated reflector. The board layout was designed with ADS and library components supplied by Siemens. The active reflector is directly bonded on the PCB shown in Fig. 22. The upper and lower two SMA connectors are used for supply and bias voltages. For each DC voltage a SMD capacitance can be soldered on to the board.



**Fig. 22. PCB layout of the test board.**

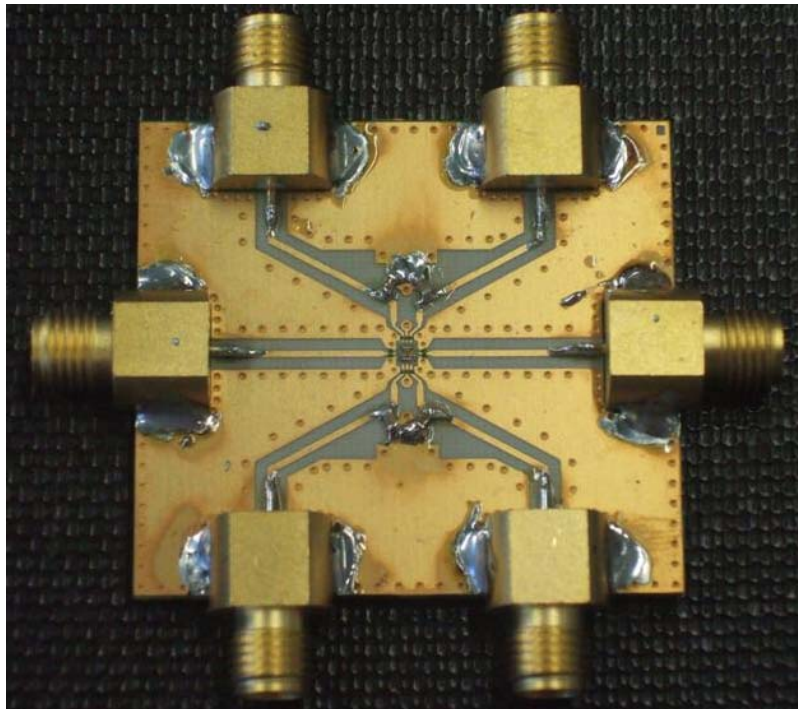


Fig. 23. PCB testboard with SMA connectors and 4 SMD capacitors.

## 6 Auto Calibration Circuit

As the measurements have shown, the oscillation frequency of the active reflector is significantly lower than it was designed for. For functionality and to be compliant to the ISM band specifications (5.725GHz – 5.875 GHz), it is important that the reflector oscillates at the correct frequency. Integrated inductances and capacitances have a large production deviation which leads to a deviation in the oscillation frequency. In our case, the oscillation frequency is only 5.4GHz, which is 7% too low. Assuming that this difference is only caused by the loop filter, the inductance and the capacitance are both 7.5% too large. Such a deviation is in the normal range of a modern CMOS process. To compensate this imprecision a calibration method has to be equipped on the ALPR reflector. Different calibration schemes are discussed in the following sections

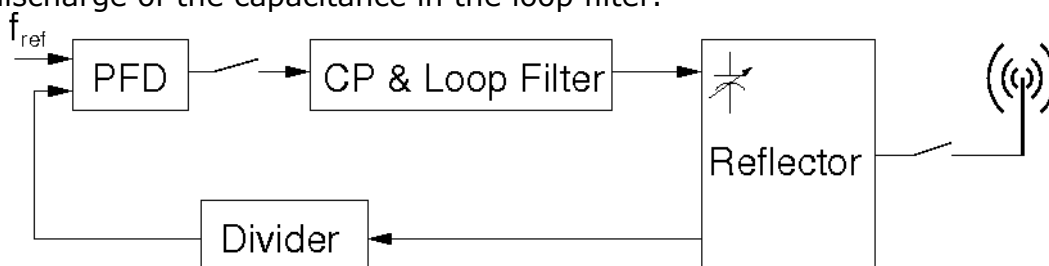
### 6.1 Comparison of different self calibration schemes

#### 6.1.1 Varactor Tuning

The simplest possibility is to tune the reflectors frequency using a varactor in the loop filter with an external control voltage. Instead of one varactor one could have multiple varactors and tune them digitally. Each reflector has then to be tuned to the right frequency and the control word could be saved permanently in a ROM. The advantage is the simplicity of the circuit. The disadvantage is that in a commercial product, the frequency cannot be tuned during operation, but only once before selling the product. This method does not compensate the variations due to temperature and the ageing of the circuit.

### 6.1.2 PLL

A PLL could be applied to the reflector in order to counterbalance the temperature and ageing effect. Before the reflector starts sending, the self calibration circuit assures operation at the right frequency. To tune the reflector, the signal has to be disconnected from the antenna. The reflector now works as an oscillator and an analogue PLL structure is build around it. As soon as the PLL is locked to the reference, the VCO control voltage has to be saved. The PLL loop is disconnected, the reflectors oscillation stopped and the antenna connected. Then the normal reflector operation starts. The disadvantages of this topology are the size and the power consumption. Furthermore, the control voltage cannot be efficiently saved in a capacitor due to leakage in the charge pump and the capacitor itself. Additional circuitry has to be used to detect the locking state and the discharge of the capacitance in the loop filter.

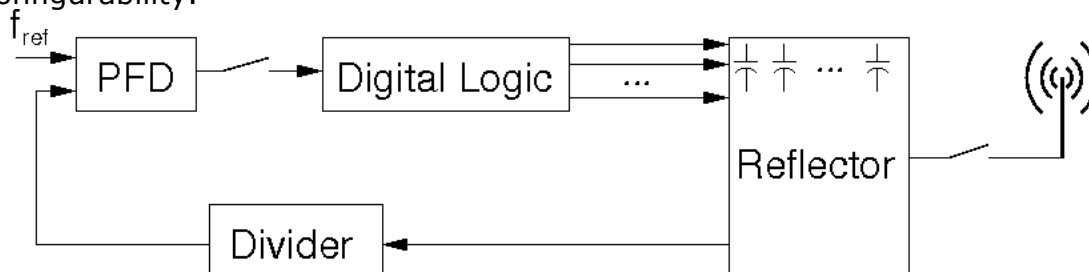


**Fig. 24. Auto calibration with an analogue PLL.**

### 6.1.3 All-digital PLL

As described in the previous subsection an analogue PLL has the disadvantage of the leaking of the capacitor. Instead of using a VCO, a digitally controlled oscillator (DCO) can be used. The ADPLL consists of a PFD, a digital control logic, which substitutes the charge pump and the loop filter, a DCO and a divider chain. The control word can be saved in registers and their states will not change over time unless the auto calibration is activated. In order to use an ADPLL in the reflector, the reflector itself has to be designed as a DCO. This can be done by using digitally tuned varactors in the loop filter of the reflector as proposed in [3].

A similar approach is to have a digitally tuneable reflector with divider chains and to compare the reference and the divided frequency with two counters implemented in an FPGA. This has the advantage of higher flexibility and reconfigurability.



**Fig. 25. Auto calibration using an all-digital PLL**

## 6.2 Comparison of Calibration Methods

	<b>Power Consumption</b>	<b>Area</b>	<b>Complexity</b>	<b>Tuneable in the field</b>
<b>Varactor Tuning</b>	small	small	small	no
<b>PLL</b>	high	high	very high	yes
<b>ADPLL</b>	medium-high	medium-high	high	yes

**Tab. 2. Comparison of four tuning methods for the active pulsed reflector**

The ADPLL is the best compromise between area, power consumption and complexity. Although the varactor tuning is simpler, it is not possible to tune the reflector after the delivery to the customer. Therefore, ageing and temperature changes cannot be compensated and it cannot be guaranteed that the reflector sends at the allowed frequency and it is insufficient for a product.

### 6.3 Concept of Auto Calibration using an ADPLL

A critical parameter is the locking time of the ADPLL. Detailed system level simulation will help to find a good calibration method using an ADPLL. At the moment two different calibration schemes are considered.

#### Fine and Coarse Tuning

When the reflector is powered up, the coarse tuning algorithm starts. The coarse tuning algorithm should compensate the production variation. This state is then saved to a register. Every time before a measurement starts, the fine tuning algorithm will be enabled. This fine tuning algorithm should only compensate the temperature variations. The idea behind splitting the fine and coarse tuning is that the calibration before the measurement is shorter.

#### Only one Tuning

The other possibility is to tune the reflector only once after the power-up. The advantage is that the calibration time can take longer. It has to be studied, if the deviation due to the temperature variation is small enough.

### 6.4 Estimated Power Consumption and Area of an ADPLL

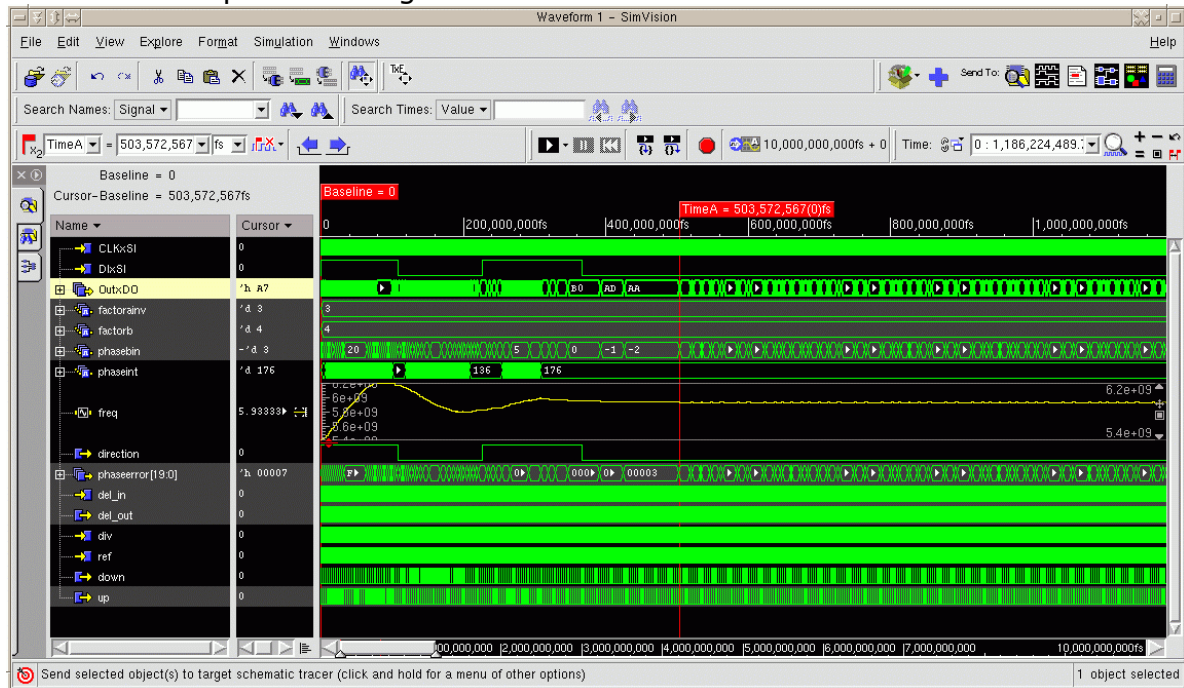
In an analogue PLL the main power dissipation is caused by the VCO and the divider. The power consumption of the divider can be reduced by using injection-locked frequency dividers (ILFD). A 5-GHz PLL with ILFDs described in [4] consumes 25mW using 1.6mm<sup>2</sup> die area in 0.24µm CMOS. The ADPLL doesn't use a large loop filter and a smaller technology will be used, thus the additional die size will be smaller.

The ADPLL needs additional external circuitry: A switch is needed between the reflector and the antenna, because the reflector is not allowed to send during calibration. Further, a reference clock is also needed.

### 6.5 First simulation results

To verify the all-digital PLL approach, the ADPLL was modelled in Verilog AMS and the digital loop filter in VHDL. A digital loop filter could be found and the functionality of the all-digital PLL approach could be verified. The locking time of the ADPLL depends on the filter bandwidth and thus also on the reference

frequency. With a reference frequency of 362MHz a locking time of 500ns could be achieved as plotted in Fig. 26.



**Fig. 26. First high-level simulations for a self calibration scheme based on an all-digital PLL. The frequency of the reflector, plotted in the middle, shows a slight over swing.**

## 7 Conclusion

In this report, a detailed analysis of the pulsed active reflector was presented. The working principle of the novel reflector approach was proven mathematically and with the help of Simulink simulations. The crucial phase coherent start-up of the reflector was thoroughly analysed and an important relation between the loop gain  $A$  and the quality factor  $Q$  could be identified. Simulink simulations of the start-up corroborated the relation between  $Q$  and  $A$ .

A suitable architecture for a pulsed active reflector was developed and implemented in silicon. The simulation results are very good. In measurement, it showed that the resonance frequency of the reflector is impacted by process variations of the loop filter. Therefore, the reflector needs to be equipped with a calibration method that allows a tuning of the oscillation frequency without any external interaction.

Such a tuning method will be implemented in the next wafer-run to prevent frequency deviations.

## 8 References

- [1] L. Wiebking, "Entwicklung eines zentimetergenauen mehrdimensionalen Nahbereichs – Navigationssystems", Düsseldorf: VDI Verlag 2003
- [2] M. Shouxian et. al., "A Modified Architecture Used for Input Matching in CMOS Low-Noise Amplifiers", IEEE Transactions on Circuits and Systems-II: Express Briefs, Vol. 52, No. 11, November 2005

- [3] R. B. Staszewski et. Al., "All-Digital Frequency Synthesizer in Deep-Submicron CMOS", John Wiley & Sons, Inc., 2006
- [4] H. R. Rategh, "S CMOS Frequency Divider with an Injection-Locked Frequency Divider for a 5 GHz Wireless LAN Receiver", IEEE Journal on Solid-State Circuits, Vol. 35, No. 5, May 2000