Low-Cost BiCMOS Variable Gain LNA at $K_{\mu}$-Band With Ultra-Low Power Consumption

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Abstract—A low-noise amplifier (LNA) at $K_{\mu}$-band with variable gain for adaptive antenna combining is presented. The compact MMIC is optimized for low-power-consuming wireless local area network applications and is fabricated using commercial 0.25-$\mu$m bipolar complementary metal–oxide semiconductor technology. At 16 GHz, a supply voltage of 1.5 V and a current consumption of only 1.5 mA, maximum gain of 14.5 dB, noise figure of 3.8 dB, and third-order intercept point at the output of 1 dBm are measured. At a supply voltage of only 1 V and a supply current of 0.9 mA, a gain of 11 dB was achieved, yielding a gain per supply power figure-of-merit of 12.2 dB/mW, which, to the knowledge of the authors, is the highest reported to date for $K_{\mu}$-band LNAs, independent of the technology used. The characteristics of different bias methods for amplitude control of the cascode circuit are elaborately discussed. A bias-control method is proposed to significantly decrease the transmission phase variations versus gain.

Index Terms—Adaptive antenna combining, bipolar complementary metal–oxide semiconductor (BiCMOS), $K_{\mu}$-band, low-noise amplifier (LNA), monolithic microwave integrated circuit (MMIC), wireless local area network (WLAN).

I. INTRODUCTION

III/V-BASED low-noise amplifiers (LNAs) with low power consumption and excellent properties in terms of gain, noise, and linearity have been reported in the past [1], [2]. Due to the strong price competition in the wireless market, minimization of circuit costs has become a mandatory design goal. Today, silicon-based circuits are preferred since, in comparison to their III/V-based counterparts, they offer low-cost transceiver solutions on a single chip. Recently, excellent results up to C-band have been reported for LNAs fabricated with commercial complementary metal–oxide semiconductor (CMOS) [3], [4].

Due to the increasing demand in terms of data rate and bandwidth, operation frequencies at $K_{\mu}$-band are proposed for wireless local area network (WLAN). One example is the high performance radio local area network (HIPERLAN) IV standard [5] in Europe, which will offer data rates of up to 155 Mbit/s. HIPERLAN IV has an allocated frequency band around 17 GHz.

With commercial low-cost technologies and at such high frequencies, it is challenging to reach satisfying performances at low power consumption. At the $K_{\mu}$-band, good gain per supply power figures of merit (FOMs) up to 1 and 3.1 dB/mW have been reached with SiGe HBTs [6]–[10] and CMOS transistors [11], respectively.

Transistors with small gatewidths can be chosen to scale down the supply current. However, at the same time, the input and output impedances of the transistors are increasing. Thus, for impedance and noise matching, inductors with large inductance values are required, which increase the resistive losses and noise. Consequently, for narrow-band LNAs, the Q factor of the inductors is important. The performance of inductors on silicon-based technologies is relatively poor [12]. A major reason is the high resistive loss of the silicon substrates. Ground shields can be used to prevent the field from penetrating into the lossy substrate, thereby significantly improving the peak quality factor [13]. Unfortunately, due to the increased parasitic capacitance to ground, the resonance frequency and, thus, the maximum operation frequency, is decreased. For that reason, ground shields are not well suited for frequencies up to the $K_{\mu}$-band. At such high frequencies, isolation layers between the inductor and substrate are more efficient since they decrease the substrate losses and, at the same time, increase the resonance frequency of the inductors.

Different techniques can be applied to reach an isolation effect [14]. In the bipolar complementary metal–oxide semiconductor (BiCMOS) technology used here, isolation trenches were positioned under the passive devices.

This study shows that, even at $K_{\mu}$-band, excellent performances can be reached with low-cost BiCMOS technology. To the knowledge of the authors, the measured FOM of up to 12.2 dB/mW is by far the highest reported to date for LNAs operating above the C-band, independent of the technology used. The FOM achieved is even higher than the one reported for leading-edge III/V technologies, which are also not competitive in terms of costs. A comparison with state-of-the-art works is shown in Table I.

Adaptive antenna combining offers a high potential to improve the performance of WLAN systems [19]. However, adaptive antenna systems have very demanding requirements in terms of the power consumption of the components because several active antenna paths have to be fed with current. More information about adaptive antenna systems can be found in the literature [1], [20].

Variable gain low-noise amplifiers (VGLNAs) can be used to adjust the amplitude of each antenna path. This has the advantage that no additional attenuator or variable-gain amplifier is required. Thus, power consumption, chip size, and costs can be minimized at the same time.

In this paper, the performances of different bias methods for gain control of the cascode LNA are elaborately compared and
discussed. A bias control method is proposed to significantly decrease the transmission phase variations versus gain, thus simplifying the control complexity for adaptive antenna systems.

II. CIRCUIT DESIGN

The VGLNA was fabricated with the IBM 6HP BiCMOS monolithic-microwave integrated-circuit (MMIC) process. This commercial foundry technology features HBTs with transit frequencies \( f_T \) up to 47 GHz and minimum noise figures (NFs) \( f_{\text{min}} \) of approximately 3 dB at 17 GHz. Due to the deep trench substrate isolation technique, high quality factors are achieved for the inductors. A typical 0.7-nH inductor has a quality factor around 15 at 17 GHz. Furthermore, the process provides metal-insulator-metal capacitors with capacitances per area of 0.7 fF/\( \mu \)m and poly resistors with resistances up to 3.6 k\( \Omega \) square. For further information concerning the MMIC process, the reader is referred to [21] and online.\(^1\) The device models of the design kit were used for the simulations.

Major goals for this work were the minimization of the power consumption, a maximum gain \( S_{21} \) above 10 dB, a high amplitude control range (maximum gain–maximum attenuation), and minimum NF. Relatively low large-signal performance can be tolerated for a short-range WLAN system, as targeted in this study.

A reactively matched cascode circuit was used to reach the design specifications. Fig. 1 shows the simplified circuit schematics of the circuit. For general LNA theory and design methodologies of bipolar cascode LNAs, the reader is referred to the literature [22]–[24].

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\( ^1\) [Online]. Available: http://www.mosis.com

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### TABLE I

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Technology/Transit freq.</th>
<th>Operation freq.</th>
<th>Ampl. control</th>
<th>( S_{21} )</th>
<th>NF</th>
<th>OIP3</th>
<th>( V_{\text{dc}} )</th>
<th>I( \text{dc} )</th>
<th>( S_{21}/P_{\text{dc}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>0.5( \mu )SiGe HBT/80GHz</td>
<td>24GHz</td>
<td></td>
<td>10dB</td>
<td>9dB</td>
<td>n.a.</td>
<td>3.6V</td>
<td>46mA</td>
<td>0.06dB/mW</td>
</tr>
<tr>
<td>16</td>
<td>0.1( \mu )SOI CMOS/100GHz</td>
<td>23.8GHz</td>
<td></td>
<td>7.3dB</td>
<td>10dB</td>
<td>0dBm</td>
<td>1.5V</td>
<td>53mA</td>
<td>0.1dB/mW</td>
</tr>
<tr>
<td>17</td>
<td>InP HEMT/100GHz</td>
<td>12GHz</td>
<td></td>
<td>17.5dB</td>
<td>1.5dB</td>
<td>n.a.</td>
<td>3V</td>
<td>20mA</td>
<td>0.3dB/mW</td>
</tr>
<tr>
<td>18</td>
<td>0.15( \mu )GaAs pHEMT/n.a.</td>
<td>30GHz</td>
<td></td>
<td>16dB</td>
<td>1.4dB</td>
<td>n.a.</td>
<td>2V</td>
<td>20mA</td>
<td>0.4dB/mW</td>
</tr>
<tr>
<td>6</td>
<td>0.5( \mu )SiGe HBT/80GHz</td>
<td>15GHz</td>
<td></td>
<td>9dB</td>
<td>4dB</td>
<td>n.a.</td>
<td>3.3V</td>
<td>7.2mA</td>
<td>0.4dB/mW</td>
</tr>
<tr>
<td>7</td>
<td>0.5( \mu )SiGe HBT/45GHz</td>
<td>12GHz</td>
<td></td>
<td>9dB</td>
<td>4.7dB</td>
<td>n.a.</td>
<td>3V</td>
<td>4mA</td>
<td>0.8dB/mW</td>
</tr>
<tr>
<td>8</td>
<td>0.5( \mu )SiGe HBT/80GHz</td>
<td>10.5GHz</td>
<td></td>
<td>26dB</td>
<td>2dB</td>
<td>n.a.</td>
<td>3.6V</td>
<td>7.4mA</td>
<td>1dB/mW</td>
</tr>
<tr>
<td>9</td>
<td>SiGe HBT/50GHz</td>
<td>16GHz</td>
<td></td>
<td>8dB</td>
<td>4dB</td>
<td>n.a.</td>
<td>1.5V</td>
<td>5.3mA</td>
<td>1dB/mW</td>
</tr>
<tr>
<td>10</td>
<td>SiGe HBT/155GHz</td>
<td>19GHz</td>
<td></td>
<td>26dB</td>
<td>2.2dB</td>
<td>n.a.</td>
<td>3V</td>
<td>8.7mA</td>
<td>1dB/mW</td>
</tr>
<tr>
<td>11</td>
<td>0.18( \mu )CMOS/n.a.</td>
<td>21.8GHz</td>
<td></td>
<td>-28dB</td>
<td>6dB</td>
<td>n.a.</td>
<td>1.5V</td>
<td>16mA</td>
<td>3.1dB/mW</td>
</tr>
<tr>
<td>2</td>
<td>0.5( \mu )MESFET/18GHz</td>
<td>5GHz</td>
<td>Switch</td>
<td>12.3dB</td>
<td>2.4dB</td>
<td>-8.3dBm</td>
<td>1V</td>
<td>1.2mA</td>
<td>10dB/mW</td>
</tr>
<tr>
<td>This work</td>
<td>0.25( \mu )BiCMOS/47GHz</td>
<td>16GHz</td>
<td>35 dB</td>
<td>14.5dB</td>
<td>3.8dB</td>
<td>1dBm</td>
<td>1.5V</td>
<td>1.5mA</td>
<td>6.4dB/mW</td>
</tr>
</tbody>
</table>

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Fig. 1. Simplified schematics of the VGLNA. \( V_{\text{ce}} \): supply voltage. \( V_{\text{be}} \): base–emitter voltage of common source circuit. \( V_{\text{bc2}} \): base voltage of common gate circuit. \( I_{\text{ce}} \): supply current.

HBTs with a small emitter area are used to scale down the supply current. However, the decrease of the emitter size is limited since the resulting increase of the input and output impedances demands matching inductors with high values. To have reasonable quality factors at 17 GHz, the required value of the inductors should be kept below a value of approximately 1 nH. Thus, the decrease of the emitter area for supply current scaling is limited. An optimum tradeoff has to be found.

The bases of the common base and common emitter circuit are biased by high ohmic resistors. A shunt capacitance is used as RF termination of the base of the common base stage. The output matching inductor is used to feed the supply current.
III. RESULTS OF LNA

The circuit was measured on wafer. All measurements were performed at source and load impedances of 50 $\Omega$ and include the losses of the pads.

Fig. 3 shows the measured and simulated gain and NF versus frequency at the bias point providing the best tradeoff between maximum gain and minimum NF. At 16 GHz, $V_{cc} = 1.5$ V, $V_{be1} = 0.95$ V, $V_{be2} = 1.5$ V, and $I_c = 1.5$ mA, a gain of 14.5 dB and a NF of 3.8 dB were measured. At this bias point, a FOM of 6.4 dB/mW is achieved. The measured input and output return losses are 4 and 18 dB, respectively. The input return loss is relatively low since the input was optimized for minimum NF rather than for high return loss. A relative low-input return loss can be tolerated for the LNA because the input is terminated by a passive antenna. Thus, there should be no problems concerning stability. A third-order intercept point at the output (OIP3) of 1 dBm is reached, which is sufficient for demanding application.

Lower large-signal performance can be accepted for short-range applications as targeted for HIPERLAN IV. Thus, the supply power can be further decreased. At 16 GHz, $V_{CC} = 1$ V, $V_{be1} = 0.9$ V, $V_{be2} = 1.35$ V, and $I_c = 0.9$ mA, a gain of 11 dB is achieved, yielding a very high FOM of 12.2 dB/mW. In this bias point, an NF of 4.1 dB and an OIP3 of $-11$ dBm were measured.

The authors believe that the FOMs achieved for both bias points are by far the highest ever reported for LNAs operating above $C$-band, independent of the MMIC technology used. A comparison with other works from $C$-band to $Ka$-band by means of the FOM versus NF is illustrated in Fig. 4.

IV. BASIC VARIABLE GAIN METHODS

The gain of the cascode LNA can be varied with one of its bias voltages. The following basic bias modes are possible.

Mode 1: Decreasing of $V_{be1}$. The two other bias voltages ($V_{be2}, V_{CC}$) are kept constant. Gain is decreased since the transconductance of the transistors is decreasing with the bias current.

Mode 2: Decreasing of $V_{be2}$. The two other bias voltages ($V_{be1}, V_{CC}$) are kept constant. Gain is decreased since the collector emitter voltage of the common emitter stage $V_{CES} = V_{be2} - V_{be1}$ is driven into the saturation region, which has resistive characteristics.

Mode 3: Decreasing of $V_{CC}$. Gain is decreased since the collector emitter voltage of the common base stage $V_{CBE} = V_{CC} - V_{be2} + V_{be1}$ is driven into the saturation region.

Generally, bias mode 3 is not recommended since a relatively high control current (collector current) has to be provided. Bias modes 1 and 2 have the advantage that their control current (base current) is very low. This lowers the requirements for the digital to analog converter, which has to provide the analog control voltages. Thus, the following investigations focus on bias modes 1 and 2.
The most important properties such as the gain, transmission phase, NF, supply current, and OIP3 were characterized versus the corresponding bias voltage and are discussed in Sections IV-A–F, respectively. The following investigations are related to an operation frequency of 16 GHz.

A. Gain Control

On the left axes of Fig. 5(a) and (b), the measured and simulated gain $S_{21}$ are plotted versus $V_{be1}$ (bias mode 1) and $V_{be2}$ (bias mode 2), respectively. The maximum attenuation is determined by the parasitic input-to-output feedback capacitance of the transistors. Due to the small size of the transistors, the values of these feedback capacitances are low. Consequently, high gain-control ranges of above 30 dB are achieved for both bias modes.

A gain-control range of approximately 10 dB is sufficient for the important antenna paths of a system and is used to compare the characteristics of the bias modes. Generally, only those antenna paths require higher attenuations, which are not significant concerning the signal quality. Thus, the variable gain performance for higher gain-control ranges are of minor relevance. For modes 1 and 2, a gain-control range of 10 dB is achieved for a variation of $V_{be1}$ from 0.9 to 0.835 V, and a variation of $V_{be2}$ from 1.35 to 0.97 V, respectively.

B. Transmission Phase

Unfortunately, the transmission phase (phase of $S_{21}$) is not constant versus gain since the $RC$ time constants of the transistors are varying with the bias.

The measured and simulated transmission phase versus control voltages of bias modes 1 and 2 are shown on the right axes of Fig. 5(a) and (b), respectively. Within a gain-control range of 10 dB, a transmission phase variation of 25° is measured for bias mode 1. The phase variation is mainly attributed to the variation of the input capacitance of the cascode stage. Over the same gain-control range, a higher transmission phase variation of 49° is measured for bias mode 2. This phase variation is generated by the strong resistive and capacitive variations occurring during the transition from the forward active to the resistive region.

C. NF

The measured and simulated NFs of the two modes are compared on the left-hand-side axes of Fig. 6(a) and (b). Over the gain-control range of 10 dB, the noise is increasing from 4.1 to 6.5 dB for bias mode 1 since the decrease of $V_{be1}$ moves the bias current away from the current for minimum noise. For mode 2 and over the same gain-control range, the noise is increasing up to 9.7 dB because the common emitter stage is driven into the resistive region.
D. Current Consumption

The supply current is falling with decreasing bias. This is advantageous since it lowers the power consumption. The corresponding performances are depicted on the right axes of Fig. 6(a) and (b). For bias modes 1 and 2 and a gain-control range of 10 dB, the measured supply current varies from 0.9 to 0.35 and 0.6 mA, respectively.

E. Return Losses

The output impedance stability of the VGLNA is important to minimize the influence on active circuits such as a phase shifter or a mixer connected with the output of the VGLNA. Large variations of the output impedance could cause performance degradations and instability of the system. Variations of the input impedance of the VGLNA are less critical because, in most cases, the input of the VGLNA is terminated with a passive antenna.

The measured and simulated return losses of bias modes 1 and 2 are shown in Fig. 7(a) and (b). Over the control range of 10 dB, the measured input return losses are higher than 4 dB for both bias modes. The measured output return losses are higher than 12.5 and 11.5 dB for bias modes 1 and 2, respectively.

F. OIP3

The OIP3 is decreasing with bias since the supply current and supply voltages are decreased, thus lowering the maximum signal amplitude of the signal at the fundamental frequency and increasing nonlinear effects.

The measured and simulated OIP3 characteristics of bias modes 1 and 2 are plotted in Fig. 8(a) and (b). Over the gain-control range of 10 dB, an OIP3 from −2 to −7 and −5 dBm were measured for bias modes 1 and 2, respectively.

V. BIAS TECHNIQUE FOR CONSTANT TRANSMISSION PHASE

It has been shown in Section IV-B that bias modes 1 and 2 have significant phase variations. However, a constant phase versus gain is mandatory for many types of adaptive antenna systems. Variations of the transmission phase could be compensated by the phase shifters within the antenna paths. Unfortunately, in this case, gain and phase could not be controlled independently. A feedback control loop would be required, which would significantly increase the control complexity. Thus, a VGLNA with constant phase versus gain is highly preferred.

A smart bias method reaching that goal is proposed here. The basic idea is that, within a given bias range, bias modes 1 and 2 have opposite phase characteristics. Decreasing of $V_{be1}$ from 0.9 to 0.825 V generates a phase drop of 30°, whereas decreasing of $V_{be2}$ from 1.55 to 1.35 V increases the phase by 30°. This has been shown in Fig. 5(a) and (b). Thus, by decreasing of $V_{be1}$ together with $V_{be2}$, the phase variations compensate for each other. The resulting transmission phase and corresponding bias voltages versus gain are plotted in Fig. 9, showing that the phase variations can be totally compensated within a gain-control range from 11 to 1 dB.
VI. CONCLUSIONS

An ultra-low power-consuming $K_{uB}$-band VGLNA has been presented. Good agreements between measurements and simulations have been achieved. The compact MMIC is fabricated using commercial 0.25-$\mu$m SiGe BiCMOS technology. A high amplitude control range is reached, making the MMIC well suited for adaptive antenna combining. Different bias methods for amplitude control have been investigated. A smart bias technique has been proposed to significantly decrease the transmission phase variations versus gain, thereby lowering the control complexity.

This paper has shown that, even at $K_{uB}$-band, excellent performances can be reached with low-cost BiCMOS technology. To the knowledge of the authors, the presented VGLNA has by far the highest gain per supply power FOMs ever reported for an LNA above the $C$-band, independent of the technology used.

The LNA is an excellent candidate for future WLAN systems, which are, for example, operating in accordance to the HIPERLAN IV standard.

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REFERENCES


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