Abstract—This paper investigates the influence of parasitic interconnections on high speed logic gates. A complementary metal oxide semiconductor logic (CMOS) gate, a high speed source coupled logic (SCL) gate and a low power SCL gate are compared. The circuits are fabricated on commercial 0.25 µm CMOS technology.

Index Terms—CMOS, SCL, gate delay, parasitic wiring.

I. INTRODUCTION

The enhancement of CMOS technology in terms of speed is primarily based on the down scaling of the gate lengths of the transistors [1]. Unfortunately, the overall device sizes and the corresponding wiring do not scale at the same amount. The parasitic capacitances and resistances of the wiring are proportional to the physical dimensions. Thus, the influence of the parasitic wiring on the speed are becoming more and more significant [2]. Today, computers and CAD programs for circuit simulation are very powerful allowing the consideration of these parasitics.

In this paper, the effects of the parasitic wiring for CMOS and SCL logic gates are investigated and compared. A commercial 0.25 µm IBM CMOS technology is used for fabrication of the circuits [3].

II. LOGIC GATES

For elaborate information concerning design concepts and optimization of CMOS and SCL gates it is referred to literature [4-7].

A. CMOS

Fig. 1a shows the used CMOS inverter topology consisting of one negative MOS (NMOS) transistor and one positive MOS (PMOS) transistor. The speed of the circuit is limited by the PMOS transistor since the hole mobility in the p-channel is smaller than the electron mobility in the n-channel. To drive the same current, the PMOS device has to be larger than the NMOS transistor thereby increasing the parasitic capacitances. A width ratio of 1:2 was chosen.

B. SCL

The used SCL inverter topology is illustrated in Fig. 1b. It is based on a differential pair amplifier. Only NMOS transistors are required. Poly silicon resistors are chosen for the loads. They have low parasitic capacitances, high sheet resistances and relative low tolerances.

Two different versions of SCL inverters are developed. One was optimized for high speed (HS SCL) and one was optimized for low power consumption (LP SCL). Major differences between these two topologies are the bias current and the values of the load resistors.

For details concerning dimensions and values of the circuit elements it is referred to TABLE I.

III. RING OSCILLATOR TEST CIRCUITS

Ring oscillator circuits can be used to determine the speed of the logic gates. Assuming equal rise and fall times, the corresponding gate delay \( \tau_g \) can be determined by means of the oscillation frequency \( f \) and the number of ring elements \( n \) [7]:

\[
\tau_g = \frac{1}{2nf} 
\]

(1)

Fig. 2 shows the circuit schematics of the two ring oscillator topologies. The circuits are a cascade of an odd number of identical inverters each driving the same load. A
number of 9 elements was chosen. The ninth element drives the output buffer, which provides isolation between the ring oscillator core and the external circuitry. The output buffer consists of a cascade of inverter circuits with a topology identical to the tested gates. Towards the output, the transistor sizes are made larger to improve impedance matching to the 50 \( \Omega \) measurement environment.

To ensure the start of the oscillation, an enable function realized as a negative or (NOR) gate is added to the ring. It prevents the circuit from locking into a condition where no oscillation can be build up.

The layouts and the chip photographs of the ring oscillators are shown in Fig. 3 and Fig. 4, respectively.

The CMOS circuit is only based on two MOS transistors. Thus, the layout can be made very compact, thereby minimizing the wiring parasitics.

The SCL gates require five elements, namely the two NMOS transistors, the two load resistances and the current source MOS transistor. The load resistances are area consuming making the layout large. Furthermore, the wiring of the SCL is more complex since it is differential. Thus, compared to the CMOS topology, we can expect a stronger influence of the parasitic wiring.

The layout of the HS SCL version is larger than for the LP SCL circuit since the HS topology has to drive more current than the LP SCL circuit. Thus, the devices and the wiring metals have to be larger.

IV. RESULTS

The simulations of the oscillation frequencies with and without considering the parasitic wiring are compared with the measurements. The corresponding results are summarized in TABLE II.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Operation</th>
<th>( f ) [MHz]</th>
<th>( \tau_g ) [( \mu )s]</th>
<th>Error^4 [%]</th>
<th>( P_g ) [( \mu )W]</th>
<th>( P_g \tau_g ) [mW ps]</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS(^1)</td>
<td>Simulated</td>
<td>1249</td>
<td>44.5</td>
<td>40</td>
<td>185</td>
<td>8.2</td>
</tr>
<tr>
<td></td>
<td>Simulated w. Parasitics</td>
<td>836</td>
<td>66.5</td>
<td>-6</td>
<td>185</td>
<td>12.3</td>
</tr>
<tr>
<td></td>
<td>Measured</td>
<td>890</td>
<td>62.4</td>
<td>0</td>
<td>150</td>
<td>9.4</td>
</tr>
<tr>
<td>LP SCL(^2)</td>
<td>Simulated</td>
<td>2114</td>
<td>26.3</td>
<td>171</td>
<td>160</td>
<td>4.2</td>
</tr>
<tr>
<td></td>
<td>Simulated w. Parasitics</td>
<td>618</td>
<td>89.9</td>
<td>-21</td>
<td>160</td>
<td>14.4</td>
</tr>
<tr>
<td></td>
<td>Measured</td>
<td>780</td>
<td>71.2</td>
<td>0</td>
<td>147</td>
<td>10.5</td>
</tr>
<tr>
<td>HS SCL(^3)</td>
<td>Simulated</td>
<td>2531</td>
<td>22.0</td>
<td>70</td>
<td>1064</td>
<td>35.2</td>
</tr>
<tr>
<td></td>
<td>Simulated w. Parasitics</td>
<td>1235</td>
<td>45.0</td>
<td>-17</td>
<td>1064</td>
<td>72.2</td>
</tr>
<tr>
<td></td>
<td>Measured</td>
<td>1493</td>
<td>37.2</td>
<td>0</td>
<td>1377</td>
<td>51.3</td>
</tr>
</tbody>
</table>

1) At optimum supply voltage of \( V_{dd} = 2V \).
2) At optimal operating point \( V_{dd} = 2V, \text{I}_{bias} = 150\mu A \).
3) At optimal operating point \( V_{dd} = 2V, \text{I}_{bias} = 1.2mA \).
4) Error referred to the measured value.

For the CMOS ring oscillator the deviation between the simulation without parasitic wiring and the measurement is 40%. When considering the wiring parasitics, the error referred to the measured value is only -6%.

As expected, the influence of the parasitic wiring on the SCL topologies is more significant than for the CMOS circuit.
Due to the more complex circuit topology, the layout of the differential SCL circuits is larger than the CMOS gate thereby increasing the parasitics. For the HS SCL, the error between the simulation not considering the parasitic wiring and the measurement is 70%. The error is reduced to -17% when the parasitic wiring is considered.

For the LP SCL ring oscillator, the deviation of 171% between the simulation not considering the parasitic wiring and the measurement is very high. When the wiring parasitics are considered, the error referred to the measured value is reduced to -21%.

The error of the LP SCL circuit for the simulation without considering the wiring parasitics is even more significant than for the HS SCL, although the HS SCL version has a larger layout than the LP SCL circuit. The corresponding form factor is approximately 2.5. The reason for that is that the HS SCL is driving load impedances, which are 8 times smaller than for the LP SCL version. Thus, the impact of the wiring on the HS SCL circuit is smaller than for the LP SCL topology.

V. CONCLUSION

The influence of the parasitic wiring on high speed logic gates has been investigated. For this task, optimized CMOS and SCL circuits have fabricated using commercial 0.25 µm CMOS technology.

Depending on the circuit topology and the corresponding layout, the wiring parasitics can have a strong impact. Especially for low power applications having high load impedances, the parasitic wiring significantly degrades the speed performance. To achieve accurate simulations, the consideration of the parasitic wiring is mandatory.

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