Silicon Design for Ultra-Wideband (UWB) Applications

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Introduction The generic term "Ultra-Wideband" was traditionally applied to communication systems using a frequency band much larger than the center frequency, like pulsed radar or baseband communication mainly developed under U.S. military classified programs. Since February 2002, this definition has been extended by the U.S. government (FCC) to commercial applications for fixed or portable devices with very low-emitted power density (> 75nW/Hz) and is strongly envisioned for future IEEE WPAN standards (802.15).

Goals This project primarily aims at designing sub-blocks for UWB communication systems and to integrate them into a single chip to enable a demonstrator. The main targets are listed below:

- Minimizing the power consumption;
- Minimizing the costs by using commercially available silicon (CMOS/BiCMOS);

Organization This project is sponsored by a KTI fund and is supervised by the IBM Zurich Research Laboratory in Rueschlikon (Switzerland). The latter is also the silicon supplier under the terms of a C^2ASE agreement with the Swiss Federal Institute of Technology in Zurich.

The first phase of the project consists in the elaboration of a specification for the considered system. The figure below shows an example of transceiver architecture that is currently evaluated. From a silicon point of view, the system is separated in two parts: the RF front-end and the baseband backend. The different sub-blocks will be individually investigated in the framework of this project.

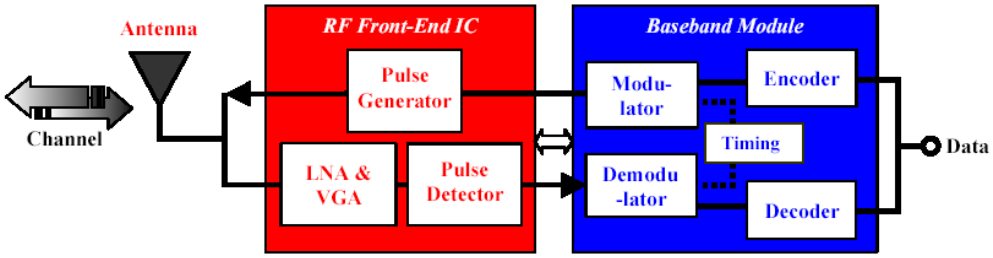

Figure 1 - Example of architecture of an UWB transceiver as considered in this project.

As an example of silicon integration, a Low Noise Amplifier (LNA) is represented in the figure below. The LNA uses serie-/shunt- feedback and peaking techniques to increase bandwidth up to 5 GHz with 13 dB gain. This LNA has been fabricated with the commercial IBM 6HP BiCMOS 0.25µ technology, which features f_T up to 47 GHz.

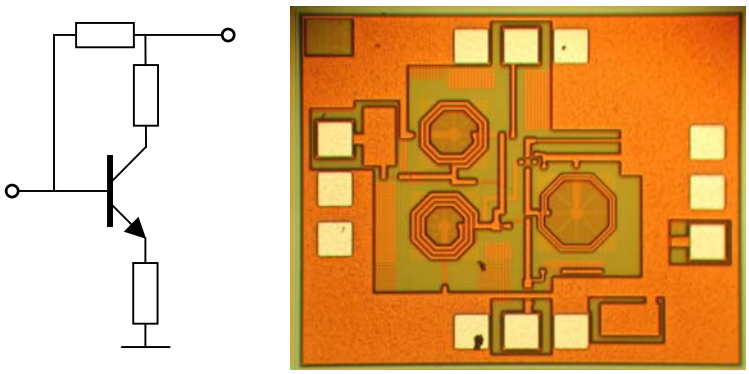

Figure 2 - Simplified AC schematics and chip photograph of the LNA (chip size: 1x 1.3 mm)