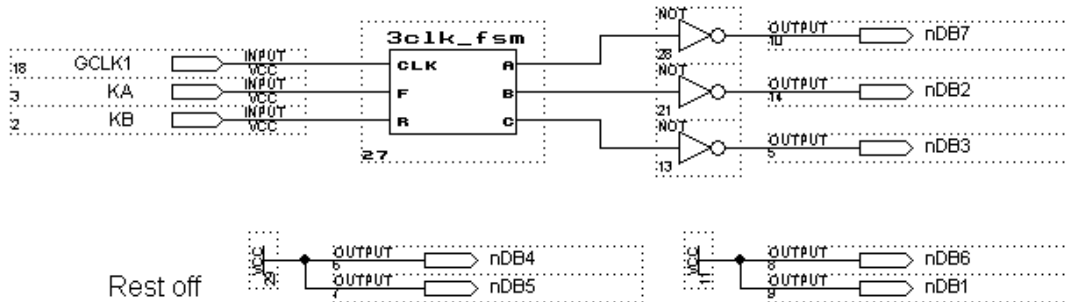


## Versuch 5: 3-Phasen Generator als AHDL-State-Machine

Beschreibung als AHDL-State-Machine als weiteres Beispiel.



### Tasten Eingabe, Anzeige mit LED

```
% 3-Phasen Clock Generator aus ELP   Zi 15.11.02 %
%
SUBDESIGN 3clk_fsm
(   CLK           : INPUT;   % Clock %
  f, r           : INPUT;   % forward, reverse %
  A, B, C        : OUTPUT;  % Phase A B C % )
VARIABLE
  SS: MACHINE WITH STATES (S0, S1, S2, S3);
BEGIN
  SS.clk = CLK;
CASE SS IS
  WHEN S0 =>
    A = GND; B = GND; C = GND;
    IF    !f&!r THEN SS = S0;
    ELSIF f&!r THEN SS = S3;
    ELSIF !f&r  THEN SS = S2;
    ELSIF f&r   THEN SS = S1;
    END IF;
  WHEN S1 =>
    A = VCC; B = GND; C = GND;
    IF    !f&!r THEN SS = S0;
    ELSIF f&!r THEN SS = S2;
    ELSIF !f&r THEN SS = S3;
    ELSIF f&r  THEN SS = S1;
    END IF;
  WHEN S2 =>
    A = GND; B = VCC; C = GND;
    IF    !f&!r THEN SS = S0;
    ELSIF f&!r THEN SS = S3;
    ELSIF !f&r THEN SS = S1;
    ELSIF f&r  THEN SS = S2;
    END IF;
  WHEN S3 =>
    A = GND; B = GND; C = VCC;
    IF    !f&!r THEN SS = S0;
    ELSIF f&!r THEN SS = S1;
    ELSIF !f&r THEN SS = S2;
    ELSIF f&r  THEN SS = S3;
    END IF;
END CASE;
END;
```

FSM Beschreibung in AHDL: 3clk\_fsm.tdf

## Report File (Auszug)

```
MAX+plus II Compiler Report File
Version 10.1 06/12/2001
Compiled: 02/11/2004 17:57:50
Copyright (C) 1988-2001 Altera Corporation
***** Project compilation was successful
```

### \*\* DEVICE SUMMARY \*\*

Chip/ POF	Device	Input Pins	Output Pins	Bidir Pins	LCs	Shareable Expanders	% Utilized
3clock	EPM3064ALC44-10	3	3	0	5	0	7 %
User Pins:		3	3	0			

### \*\* RESOURCE USAGE \*\*

Logic Array Block	Logic Cells	I/O Pins	Shareable Expanders	External Interconnect
A: LC1 - LC16	0/16( 0%)	1/ 8( 12%)	0/16( 0%)	0/36( 0%)
B: LC17 - LC32	0/16( 0%)	1/ 7( 14%)	0/16( 0%)	0/36( 0%)
C: LC33 - LC48	2/16( 12%)	3/ 8( 37%)	0/16( 0%)	2/36( 5%)
D: LC49 - LC64	3/16( 18%)	3/ 7( 42%)	0/16( 0%)	4/36( 11%)

### \*\* EQUATIONS \*\*

```
GCLK1 : INPUT;
KA : INPUT;
KB : INPUT;
```

```
-- Node name is 'nDB2'
```

```
-- Equation name is 'nDB2', location is LC041, type is output.
```

```
nDB2 = LCELL( _EQ001 $ VCC);
_EQ001 = _LC049 & _LC050;
```

```
-- Node name is 'nDB3'
```

```
-- Equation name is 'nDB3', location is LC051, type is output.
```

```
nDB3 = LCELL( _EQ002 $ VCC);
_EQ002 = !_LC049 & _LC050;
```

```
-- Node name is 'nDB7'
```

```
-- Equation name is 'nDB7', location is LC046, type is output.
```

```
nDB7 = LCELL( _EQ003 $ VCC);
_EQ003 = _LC049 & !_LC050;
```

```
-- Node name is '|3clk_fsm:27|SS~1' from file "3clk_fsm.tdf" line 8, column 4
```

```
-- Equation name is '_LC049', type is buried
```

```
_LC049 = DFFE( _EQ004 $ KB, GLOBAL( GCLK1), VCC, VCC, VCC);
_EQ004 = KA & !KB & _LC049 & !_LC050
# !KA & KB & _LC049 & !_LC050
# KA & !_LC049 & _LC050;
```

```
-- Node name is '|3clk_fsm:27|SS~2' from file "3clk_fsm.tdf" line 8, column 4
```

```
-- Equation name is '_LC050', type is buried
```

```
_LC050 = DFFE( _EQ005 $ VCC, GLOBAL( GCLK1), VCC, VCC, VCC);
_EQ005 = KA & KB & !_LC050
# !KA & _LC049 & _LC050
# !KB & !_LC049 & _LC050
# !KA & !KB;
```

```
-- Shareable expanders that are duplicated in multiple LABs:
```

```
-- (none)
```